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LOGICAL EFFORT BASE ADDER CIRCUITS TRANSISTOR SIZING USING CONSTRICTION FACTOR AND MUTATIVE VARIANTS OF PARTICLE SWARM OPTIMIZATION ALGORITHM

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AUTHOR'S DECLARATION

I declare that the work in the thesis was carried out in accordance with the regulations of Universiti Teknologi MARA. It is original and is the result of my own work, unless otherwise indicated or acknowledged as referenced work. This thesis has not been submitted to any other academic institution or non-academic institution for any degree of qualification.

I, hereby, acknowledge that I have been supplied with the Academic Rules and Regulations for Post Graduate, Universiti Teknologi MARA, regulating the conduct of my study and research.

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ABSTRACT

In Semiconductor world, the design and fabrication of Integrated Circuit (IC) associated with development time, operating speed and power requirements. The goodness of each design must be evaluated before it is chosen, especially on speed of the circuits where it represent the time taken to execute a specific function or most commonly known as delay. Conventional methods use repetitive manual testing guided by Logical Effort (LE). LE provides an easy way to compare and select circuit topologies, choose the best number of stages for path and estimate path delay. The proposal of Particle Swarm Optimization (PSO) with constriction factor (PSO-CF) and mutative variants (PSO-M) presented in this thesis attempts to create an automated process of transistor sizing optimization. The method attempts to get the target circuit delay on tested circuit's critical path based on LE calculation that accepts generated transistor size by both PSO variants as inputs to fitness function. The optimization of the transistor size will stop if maximum iteration reached of different between PSO's found delay and objective delay is very small (near or similar to '0'). Various parameters, such as swarm size and iterations were tested under different initial positions to verify PSO's performance on a adder circuits namely modified half-adder (M-HA), modified full-adder (M-FA) and modified ripple-carry adder (M-RCA). The experiments reported in this thesis showed that both PSO variants were efficient to automatically find the optimum transistor size with solution range of $[10^{-2}, 10^{-15}]$ for PSO-CF and $[10^{0}, 10^{-16}]$ for PSO-M.

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